Coil Driver Printed Circuit Board Assembly Characterization Test Report
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OBanos Engineering Consulting
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1. INTRODUCTION.

OBanos Engineering Consulting (Consultant) designed a coil driver printed circuit board assembly (PCBA) for (Client) per requirements in the document titled “Low Noise Coil Driver”, dated August 17, 2021. Each PCBA had two identical coil driver channels.
In an effort to meet these requirements, the Consultant designed into the PCBA various power supply and grounding options. The Consultant built three PCBAs to experiment with these options and find the configuration producing the a drive current waveform with the required dynamic and noise characteristics. This report summarizes those configurations and their results.

2. METHOD.

2.1 Unit Under Test (UUT).
Coil Driver PCBA part number LL0008 Revision 3, quantity = 3. The power supply and ground connections in these PCBAs were as follows:

Board S/N	Low Voltage Supply	Ground Connections	Gain (Iout/Vin)
1	External	Local (Star)	2A/V
2	Built-in	Local (Star)	0.67A/V
3	External	External	2A/V

Table 1. Power Supply and Ground connections.

The figures in the Appendix A-1 show the power and ground connections described in Table 1.
The 3 PCBAs were built per 3 different Bills of Materials (BOMs) to test the effect of the component values on the signal integrity and noise. The table in the Appendix A-2 shows these BOM differences, and the figures in the Appendix A-3 show the corresponding schematic red-lines.

2.2 Equipment and Materials.

2.2.1. DSD TECH SH-G01A USB Isolator with ADUM3160 Chip 12M.
2.2.2. KORAD KD3005D Precision Variable Adjustable 30V, 5A DC linear power supply.
2.2.3. MATRIX MPS-3010D Precision Variable Adjustable 30V 10A Linear power supply.
2.2.4. TEKPOWER TP5003D-3 Precision Variable Triple Output, 0-50V, 0-3A DC linear power supply,
2.2.5. Analog Discovery ADP3250 2-channel, 14-bit 55 MHz digital storage oscilloscope with arbitrary waveform generator.
2.2.6. Fluke 3 ½ digit73III Digital Multimeter.
2.2.7. OBanos Engineering Consulting Matched Impedance Amplifier with x10 gain.
2.2.8. Loh Labs' test coils.
2.2.9. 6” x 12” x 1/4” 6061-T6 aluminum sheet, for heat sinking.
2.2.10. Thermal compound, Chip Quik TC3-3.5G.

3. Procedure.

3.1 Setup.

Attach the UUT's power amplifiers and sense resistors to the heat sinking plate
Connect the UUT's power supplies as shown in Figure 1 in the Appendix B. Make the +30V supply dashed line connection in Board IDs 1 and 2 only.
Setup the DMM in DC current-measurement mode. Connect the test coil to the UUT through the DMM. See Figure 2 in Appendix B.
Make sure the UUTs power amplifiers are disabled by shorting their ENABLE input to GND before powering up the UUT.

3.2. Signal chain verification.

Connect the waveform generator's output to the SP IN BNC of the UUT's channel under test.
Set the waveform generator output to 100 mV peak, 0DC offset, 2.5Hz, 0.125% duty cycle pulse.
Use the oscilloscope to verify the presence of a pulse at the following test points:

SET1/2 (TP2/TP12);
ICOIL1/2 (TP25/TP11);
MON1/2 (TP7/TP16);
DVT1/2 (TP1 / TP10).

Disable the power amplifier of the channel under test by shorting its ENABLE input to GND.
Move the waveform generator's output to the SP IN BNC of the UUT's next channel under test.
Connect the test coil terminals to the other channel's coil connector.
Enable the power amplifier of the channel under test by letting its ENABLE input float.
Use the oscilloscope to verify the presence of a pulse at the channel's test points indicated previously.

3.3. Rise time measurements.

3.3.1. 3A peak current pulse.

Adjust the waveform amplitude to generate a 3A peak current through the coil, as follows:

BOARD ID 1	1.5V peak
BOARD ID 2	4.5V peak
BOARD ID 3	1.5V peak

Enable the function generator output.
Enable the power amplifier of the channel under test by letting its ENABLE input float.
Monitor the waveform at the ICOIL test point. Measure and record the rise time.
Disable the power amplifier by shorting its ENABLE input to GND.
Remove the waveform generator from the UUT first channel's SP BNC and connect it to the second channel under test.
Repeat the measurements above.

3.3.2. 6A peak current pulse.

Adjust the waveform amplitude to generate a 6A peak current through the coil, as follows:

BOARD ID 1	3V peak
BOARD ID 3	3V peak

Enable the waveform generator output.

Enable the power amplifier of the channel under test by letting its ENABLE input float.
Monitor the waveform at the ICOIL test point. Measure and record the rise time.
Disable the power amplifier by shorting its ENABLE input to GND.
Repeat for both UUT channels.
For BOARD ID 2 only: (This is necessary because the Analog Discovery waveform generator maximum output is 5VDC and we need 9VDC to drive 6A through the coil)
Connect the waveform generator output to the Matched Impedance Amplifier input BNC.
Connect the Matched Impedance Amplifier "Full" test point to the SP BNC of the UUT's channel under test.
Set the waveform generator output to 900mV peak.
Enable the function generator output.
Enable the power amplifier of the channel under test by letting its ENABLE input float.
Monitor the waveform at the ICOIL test point. Measure and record the rise time.
Disable the power amplifier by shorting its ENABLE input to GND.
Repeat for both UUT channels.

3.3. Noise measurements.

3.3.1. Test Condition #1: Setpoint connected to GND; coil current = 0A.

Connect the SP test point of the UUT's channel under test to a PCBA GND test point.
Enable the power amplifier of the channel under test by letting its ENABLE input float.
Monitor the waveform at the ICOIL test point.
Measure the waveform's AC RMS value. Record the FFT plot. Window = Hamming. Span = 0.2Hz to 300 kHz.
Monitor the waveform at the DVT test point.
Measure the waveform's AC RMS value. Record the FFT plot. Window = Hamming. Span = 0.2Hz to 300 kHz.
Disable the power amplifier by shorting its ENABLE input to GND.
Repeat for the next UUT channel.

3.3.2. Test Condition #2: Setpoint connected to Waveform Generator; coil current = 1A DC.

Connect the waveform generator output to the SP BNC of the UUT's channel under test.
Adjust the waveform amplitude to generate a 1A DC current through the coil, as follows:

BOARD ID 1	0.5V DC
BOARD ID 2	1.5V DC
BOARD ID 3	0.5V DC

Enable the power amplifier of the channel under test by letting its ENABLE input float.
Monitor the waveform at the ICOIL test point.
Measure the waveform's AC RMS value. Record the FFT plot. Window = Hamming. Span = 0.2Hz to 300 kHz.
Monitor the waveform at the DVT test point.
Measure the waveform's AC RMS value. Record the FFT plot. Window = Hamming. Span = 0.2Hz to 300 kHz.
Disable the power amplifier by shorting its ENABLE input to GND.
Repeat for the next UUT channel.

4. RESULTS

4.1. Signal chain verification.

The PCBAs 001 and 002 met the signal chain verification test goals. The PCBA SN003's channel 1 stopped driving current to the coil after a few minutes of operation and did not recover.

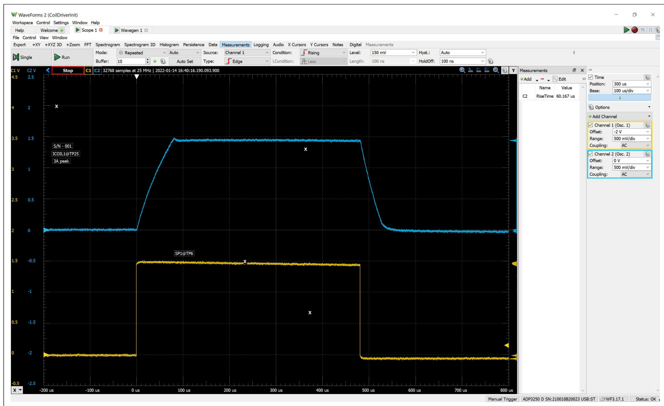
4.2. Rise time measurements, 3A peak.

ID	ICOIL1@TP25	ICOIL2@TP11
SN-001	60.167 us	99.38 us
SN-002	46.25 us	47.9 us
SN-003	N/A	105.8 us

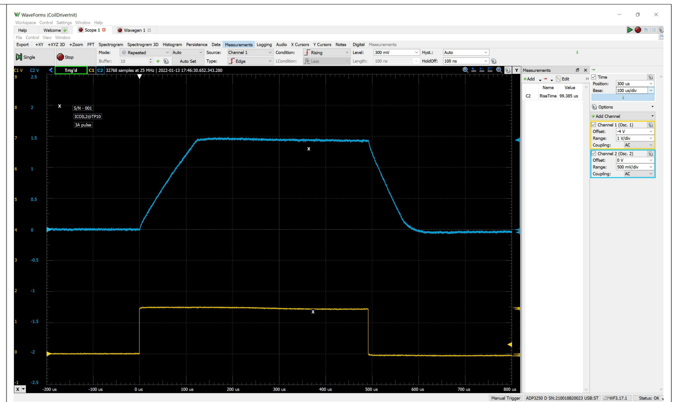
4.3. Waveforms, 3A peak.

Note: For each channel, the component values that affect the signal rise -time are listed below each oscilloscope screen capture.

4.3.1. S/N -001

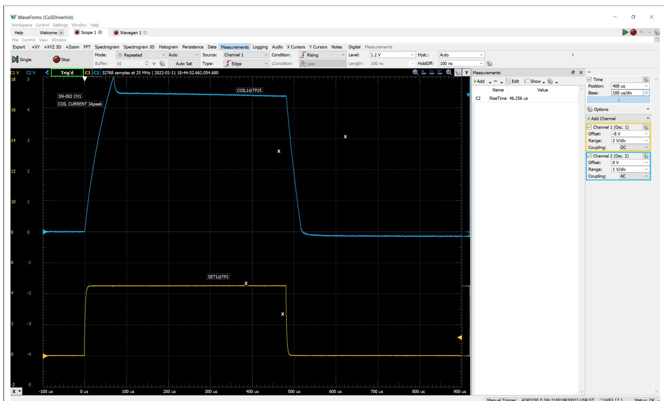


CH1. R2, R10 = 1k; R3 = 1M; R1 = 50k; C16 = 1nF; C13 = 22nF; R9 = DNI.

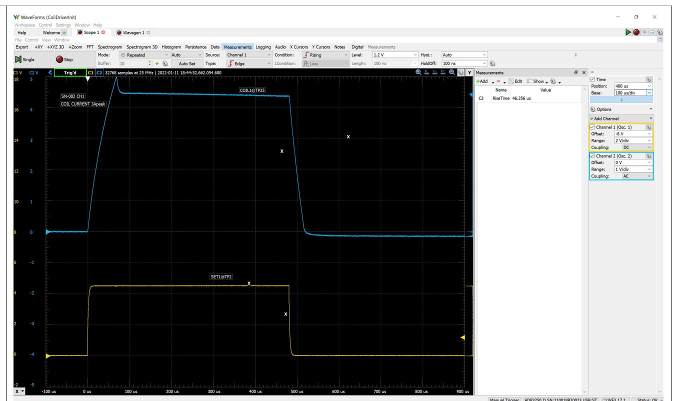


CH2. R43, R63 = 1k; R42 = 50k; C76 = 22nF; C66 = 22nF; R51 = DNI.

4.3.2. SN – 002

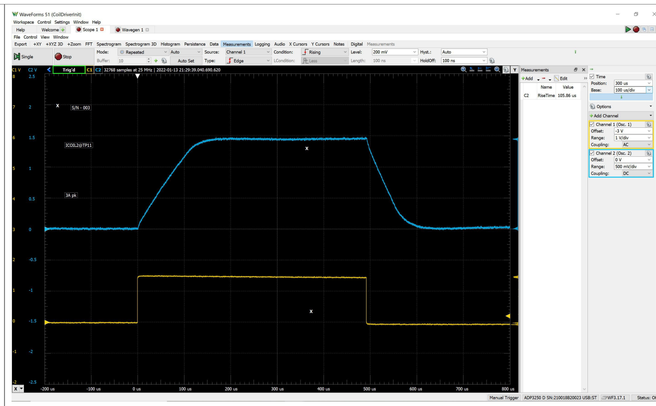


CH1. R2 = 0R; R10 = 3.01k; R1 = 100k; C16 = 22nF; C13 = 1nF; R9 = 3.01k



CH2. R43 = 0R; R63 = 3.01k; R42 = 100k; C76 = 22nF; C66 = 1nF; R51 = 3.01k.

4.2.1. 4.3.3. SN – 003

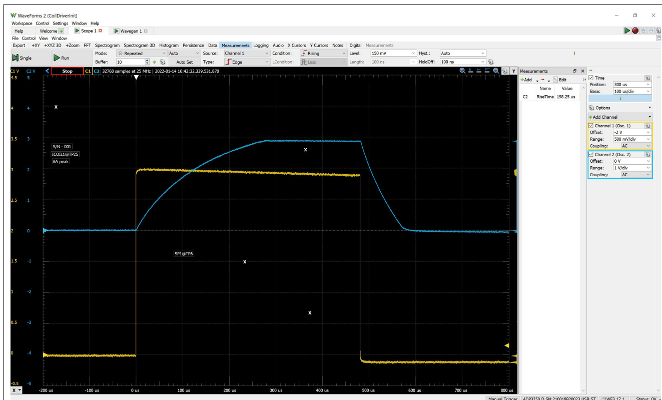
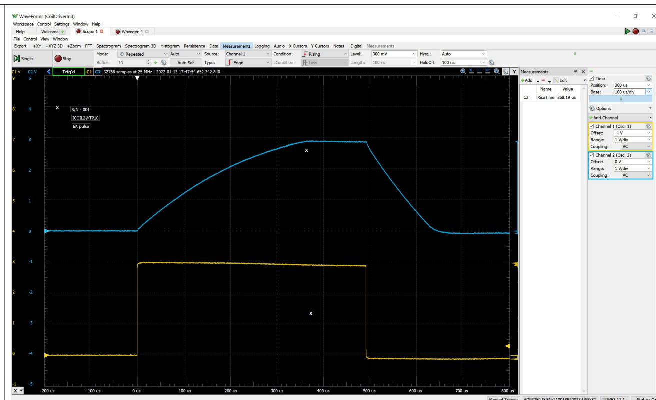
Not Available CH1	 **CH2**. R43, R63 = 3.01k; R42 = 100k; C76 = 22nF; C66 = 1nF; R51 = DNI.

4.4. Rise time measurements, 6A peak.

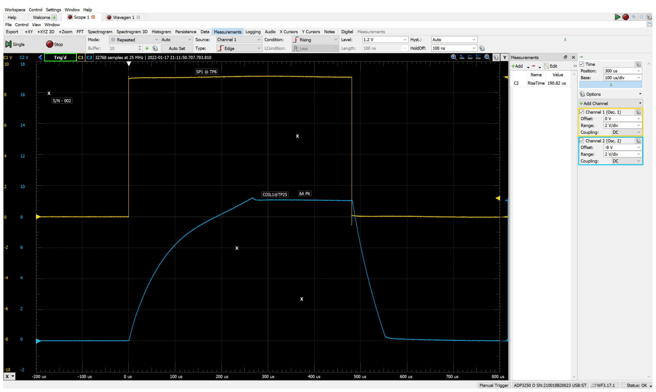
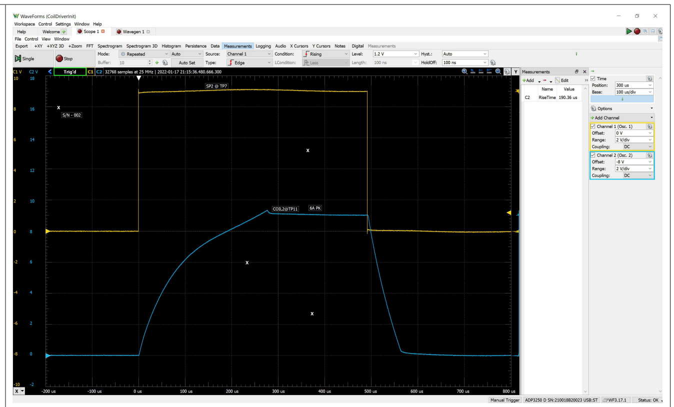
ID	ICOIL1@TP25	ICOIL2@TP11
SN-001	198.25 us	268.19 us
SN-002	190.8 us	190.4 us
SN-003	N/A	300 us

4.5. Waveforms, 6A peak.
Note: For each channel, refer to the component values in section 4.3.

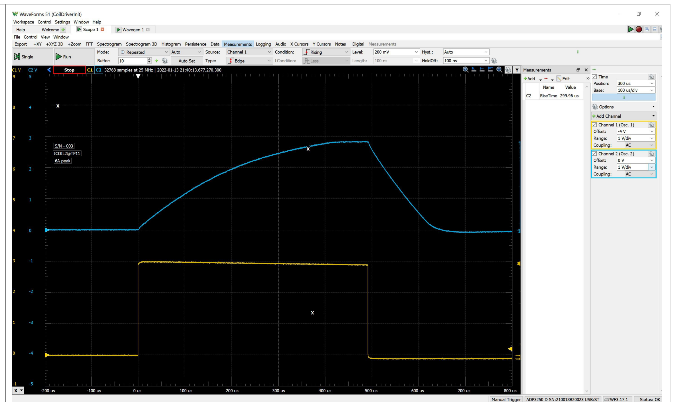
4.5.1. SN – 001

 CH1	 CH2

4.5.2. SN – 002

 CH1	 CH2

4.5.3. SN – 003

Not Available CH1	 CH2

4.6. Noise Measurements.

Note 1. All voltage measurement units are AC rms.

Note 2. The test points ICOIL1 (TP25) and ICOIL2 (TP10) have a trans-impedance (Vout / Isense) of:

PCBAs S/N -001 and S/N – 003 = 0.5V / A;

PCBA S/N – 002 = 1.5V / A

Note 3. The test points DVT1 (TP1) and DVT2 (TP10) have a trans-impedance (Vout / Isense) of 303mV / mA for all boards.

4.6.1. Coil current = 0.

S/N	ICOIL1		ICOIL2		DVT1		DVT2	
	Raw meas.	Equivalent current noise	Raw meas.	Equivalent current noise	Raw meas.	Equivalent current noise	Raw meas.	Equivalent current noise
1	136.8 uVrms	273.6 uArms	135.7 uV	271.4 uArms	2.88 mV	9.5 uArms	1.99 mV	6.5 uArms
2	173.6 uVrms	115.73 uArms	138 uV	92 uArms	3.7 mV	12 uArms	3.85 mV	12.7 uA rms
3	N/A	N/A	137 uV	274 uArms	N/A	N/A	8.7 mV	28.7 uArms

4.6.2. Coil current = 1ADC.

S/N	ICOIL1		ICOIL2		DVT1		DVT2	
	Raw meas.	Equivalent current noise	Raw meas.	Equivalent current noise	Raw meas.	Equivalent current noise	Raw meas.	Equivalent current noise
1	168.63 uVrms	337.26 uArms	175.88 uVrms	351.76 uArms	49.6 mVrms	163 uArms	39.54 mVrms	130 uArms
2	181 uVrms	120.6 uArms	179 uVrms	119.3 uArms	18.05 mVrms	59 uArms	20.22 mVrms	66.7 uArms
3	N/A	N/A	163 uVrms	326 uArms	N/A	N/A	44.25 mVrms	146 uArms

4.7. Noise Measurement waveforms.

The Appendix C shows the noise waveforms for PCBA S/N -002.

5. DISCUSSION

5.1. Power supply considerations.

The boards require the OPA549 power amplifier to be **disabled** in order to power up. Otherwise they draw excess current from the power supplies and cause them to clamp the output voltage below its target value. The current overload occurs because the PI amplifier output swings to the supply rail immediately after power is applied to the board. This forces the power amplifier to drive a full-scale current to the test coil. Since the OPA549 filter capacitors are not yet fully charged, the output current spike is drawn from the bench top power supply, causing the overload condition.

The board powers up normally as long as the OPA549 remains disabled during this period.

5.2. PCBA -003 functional failure.

5.3. The power amplifier IC3 was irreparably damaged. A potential explanation for the failure is as follows: Consultant connected the power amplifier's local ground plane to the +30V power supply return only, as requested by Client in the Coil Driver requirements specification document. The component's -30V supply return was not connected to the +30V power supply return.

The lack of a common return for the +/-30V supplies may have caused them to drift away from one another and to exceed the OPA549's supply voltage differential absolute maximum rating, thus damaging the part.

To prevent further damage, Consultant connected all returns together at the power supplies before continuing to test this board.

5.4. Output current waveform.

The measurements show that PCBA S/N 002 exhibits the shortest rise times and the largest amount of overshoot when driving a 3A pk pulse to the coil. The 6A peak transient is largely

limited by the OPA549 slew rate specification.
The waveform rise time and percent overshoot depend on the circuit's trans-conductance Iout/Vin (overshoot), and the power amplifier's bandwidth (rise time). The table below shows the results of circuit simulations and how these components affect the shape of the output current waveform – and its noise performance.

PCBA SERIAL NUMBER	CF_OPA549	CF_PI	Iout / Vin	risetime (1A out) (us)	Noise 0.2Hz – 300kHz (uVrms)
-001 CH2	22N	22N	2	17	9.5
-003, BOTH CHANNELS	1N	22N	2	15	11.8
-001 CH1	22N	1N	2	11	9.8
NONE	1N	1N	2	9.5	12
NONE	22N	22N	0.67	18	3.42
-002, BOTH CHANNELS	1N	22N	0.67	10	4.22
NONE	22N	1N	0.67	17	3.52
NONE	1N	1N	0.67	11	4.33

Table 1. Theoretical rise time and rms noise values for various PCBA component combinations.

5.4. Noise measurements.

The noise measurement data for both test conditions (coil current = 0 and coil current = 1A DC) point to the configuration in PCBA S/N -002 as the lowest noise configuration. This is in agreement with the predicted noise simulations presented in Table 1.
The circuit used to measure the output current noise suffers from practical limitations. Consider for example the following data, taken from PCBA S/N -002:

S/N – 002		
Test condition (Coil 1)	ICOIL2(TP25)	Equivalent current noise
Rsense shorted	138 uVrms	92 uArms
Rsense open. SP1 tied to GND.	173.6 uVrms	115.73 uArms
Coil current = 1A DC	181 uVrms	120.6 uArms

With the sense resistor shorted, the coil current instrumentation amplifier (INA) (which has a gain of x3) reports a voltage noise measurement of 138 uVrms, equivalent to a noise current measurement of 92 uA rms. This is obviously the noise floor of the measurement system, in this case, the instrumentation amplifier.
When the output current measures 1A DC, the equivalent current noise measurement equals 120.6 uArms. Because the INA noise and the current noise are uncorrelated, one could calculate the actual AC rms noise current X (measured by this system) as
X = sqrt (120.6^2 – 92^2) = <u>78 uArms</u>.

For this test condition (PCBA S/N – 002 driving 1ADC to the coil) the FFT shows a maximum noise level of -109 dBV over the bandwidth from 0.2Hz to 300 kHz equivalent to 3.548 uVrms, or 2.36 uArms.

While the absolute noise value may be obscured by the uncertainty in the measurement system, it seems clear that the S/N -002 configuration produces better results that its counterparts.

Additional points regarding the PCBAs output current operation and performance:

- The RMS noise increases with temperature, with the measurements changing from around 170 uVrms to approximately 190 uVrms over a period of 1 minute of driving 1A DC to the coil.
- The OPA549 enters thermal shutdown at output current levels greater than 2A DC. Obviously the aluminum plate being used as a heat sink is insufficient to dissipate the heat away from the part. Using a fan is detrimental to the PCBA's noise performance, which Consultant assumes is due to thermal changes resulting from the air blown over the part.
- As mentioned previously, removing a signal source from the input BNC results in the power amplifier drawing excessive current from the supply causing it to switch to current-limit. The power amplifier needs to be disabled before making any changes to the setup.

6. CONCLUSIONS AND RECOMMENDATIONS.

Based on the test results, the Consultant concludes that the PCBA circuit design meets the Client's requirements without having to make any changes to the PCB layout. When deployed, the power component's heat dissipation will have to be managed properly for optimal noise performance.

Consultant also concludes that the absolute noise measurements may be inaccurate due to the nature of the on-board measurement circuit. However, Consultant asserts the circuit configuration in PCBA S/N -002 (star ground, on-board analog supply, higher trans-conductance) is best suited for use because it produces faster transitions and lower output noise than the other two PCBAs. Consultant recommends changing all boards BOM to match the PCBA S/N -002 configuration.

Consultant's test results indicate that being able to enable / disable the power amplifier OPA549 is a requirement for proper circuit operation. Consultant recommends applying an external DC voltage (3 to 15VDC) to the headers ES1 / ES2 to disable the OPA549s when not in use.

OBanos Engineering Consulting appreciates the opportunity of working for Loh Labs in this very interesting project. We're proud of offering our specialty services in Analog / Digital Electronics Design and would be pleased to collaborate in a future project. Best wishes in your future endeavors!

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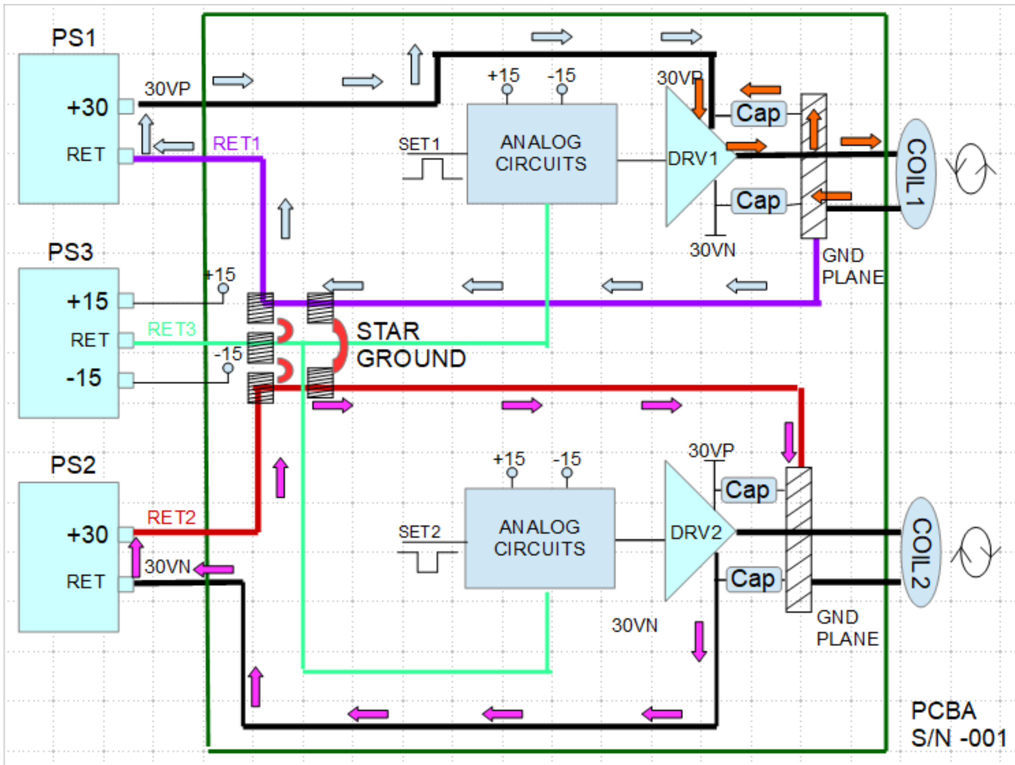
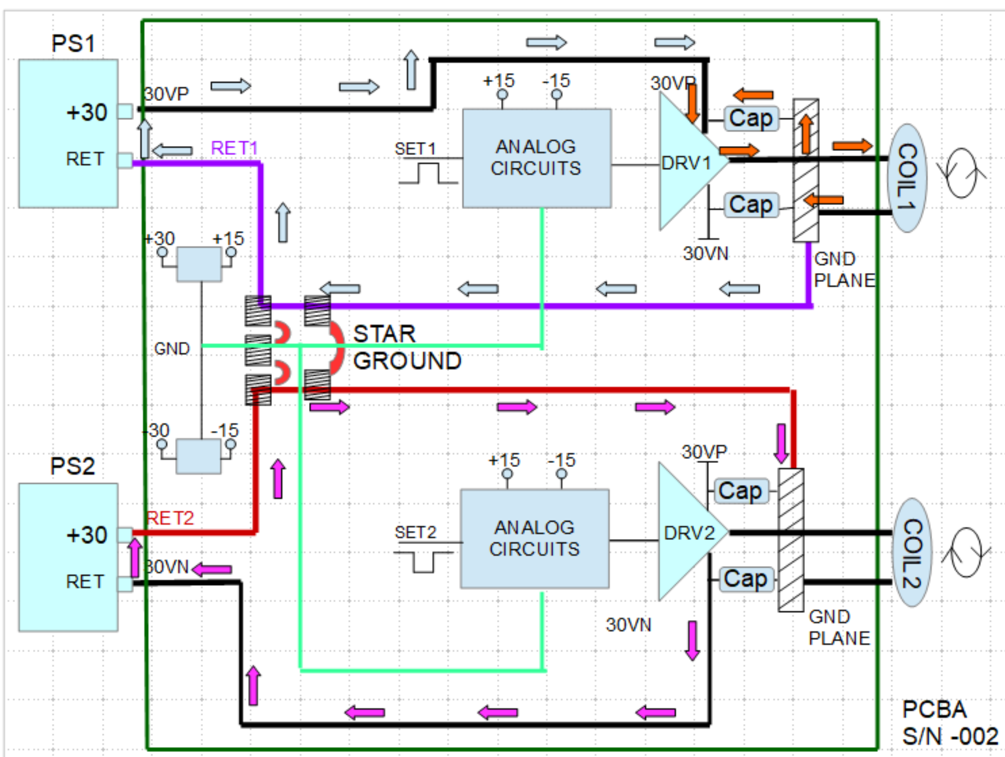
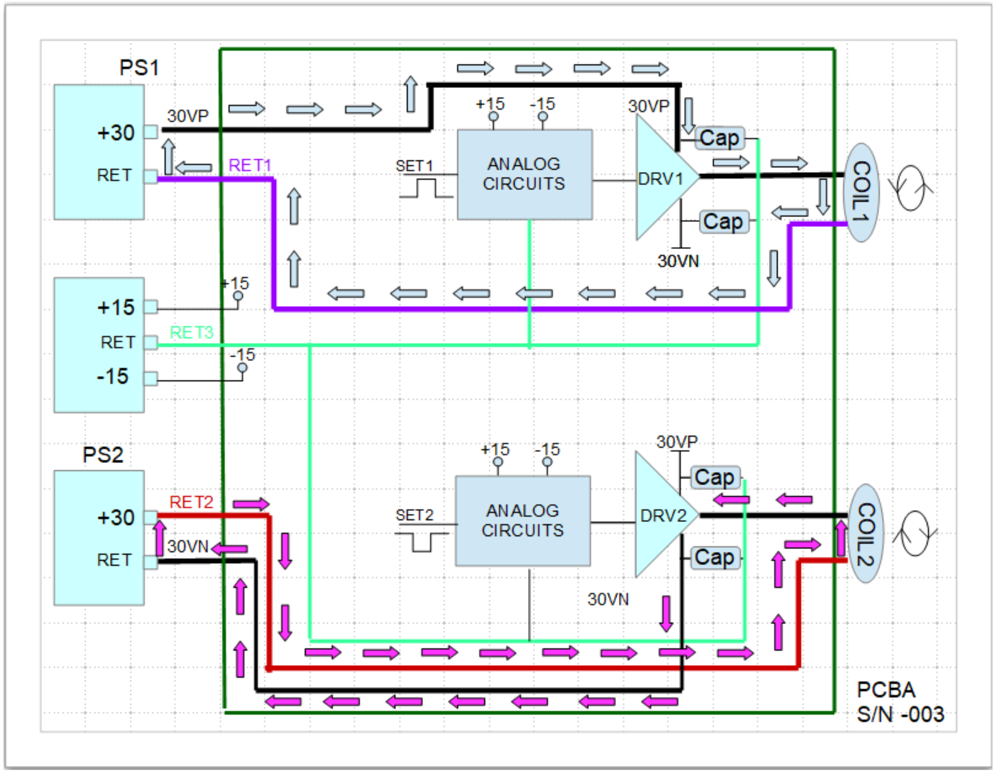
APPENDIX A-1
Power supply and ground connections for each of the 3 PCBAs.



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+30
RET
30VP
RET1
+15
-15
SET1
ANALOG CIRCUITS
30VP
Cap
DRV1
Cap
30VN
COIL 1
+15
RET
-15
RET3
PS2
+30
RET
RET2
30VN
+15
-15
SET2
ANALOG CIRCUITS
30VP
Cap
DRV2
Cap
30VN
COIL 2
PCBA
S/N -003

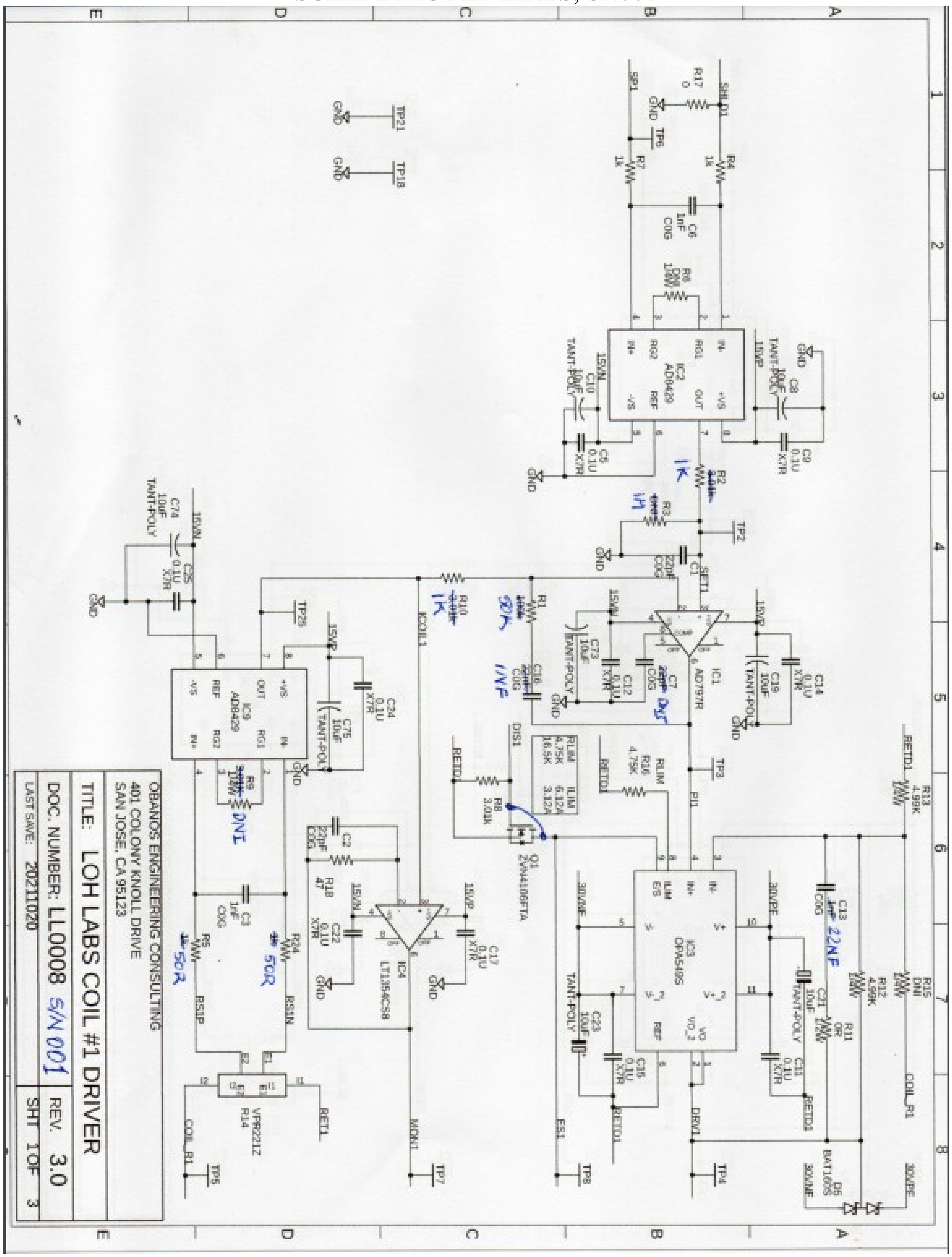
APPENDIX A-2
BOM differences between the 3 PCBAs under test

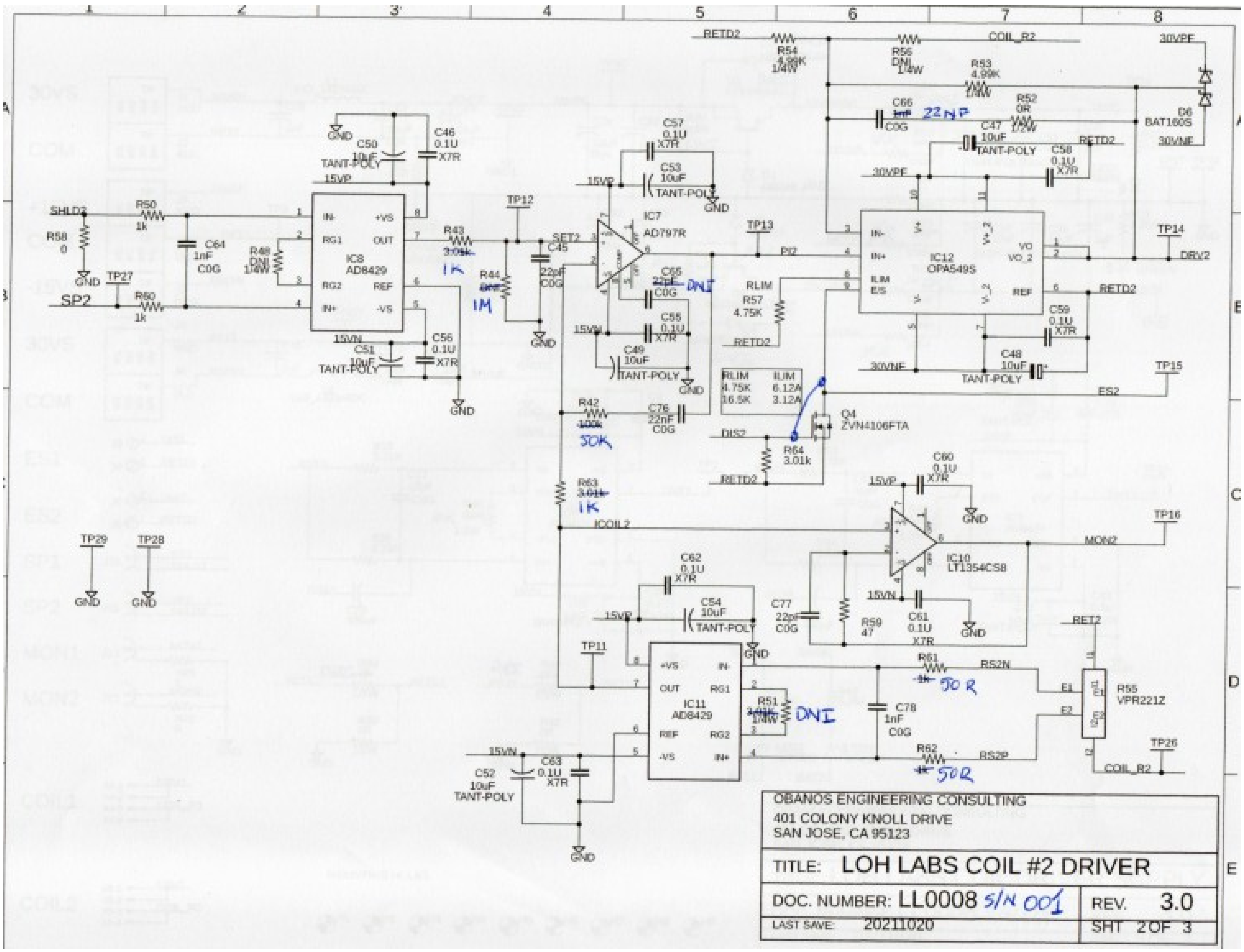
CHANNEL 1 COMPONENTS				CHANNEL 2 COMPONENTS				FUNCTION
REF DES	**S/N -001**	**S/N -002**	**S/N -003**	**REF DES**	**S/N -001**	**S/N -002**	**S/N -003**	
C16	1 NF	22 NF	22 NF	**C76**	22 NF	22 NF	22 NF	PI amplifier time constant
C13	22 NF	1 NF	1 NF	**C66**	22 NF	1 NF	1 NF	OPA549 compensation
C1	22PF	DNI	22PF	**C45**	22PF	DNI	22PF	PI amplifier input filter
R1	50K	100K	100K	**R42**	50K	100K	100K	PI amplifier time constant
R2	1K	0R	3.01K	**R43**	1K	0R	3.01K	PI amplifier input filter
R3	1M	DNI	DNI	**R44**	1M	DNI	DNI	PI amplifier input filter
R10	1K	3.01K	3.01K	**R63**	1K	3.01K	3.01K	PI amplifier gain
R9	DNI	3.01K	DNI	**R51**	DNI	3.01K	DNI	Current sense INA gain
IC1	AD797	AD797	AD797	**IC7**	AD797	AD797	AD8021	PI amplifier
Q1	ZVN4116	DNI	DNI	**Q4**	ZVN4116	DNI	DNI	OPA549 enable switch
C7	DNI	DNI	22PF	**C65**	DNI	DNI	22PF *	PI amplifier compensation
R24, R5	50R	50R	50R	**R61, R62**	50R	50R	50R	Isense INA input resistors

POWER SUPPLY COMPONENTS				FUNCTION
REF DES	**S/N -001**	**S/N -002**	**S/N -003**	
R39, R41	0 Ohm	0 Ohm	DNI	OPA549 local return jumper to Star GND
R38, R40	DNI	DNI	0 Ohm	OPA549 local return jumper to external supply
Q2	DNI	FZT1051	DNI	+15V regulator IC
Q3	DNI	FZT1151	DNI	-15V regulator IC
R20, R21	DNI	1.2 K	DNI	+/-15V regulator Zener diode bias
D2, D4	DNI	MBR0530	DNI	+/-15V discharge Schottky diode
D1, D3	DNI	DDZ16	DNI	+/-15V regulator Zener reference diode
R25	DNI	0 Ohm	DNI	+15V local regulator output jumper
R19	0 Ohm	DNI	0 Ohm	+15V external supply output jumper
R27	0 Ohm	0 Ohm	DNI	Star GND to analog ground jumper
R28	0 Ohm	DNI	0 Ohm	+/-15V external supply return jumper
R29	DNI	0 Ohm	DNI	-15V local regulator output jumper
R30	0 Ohm	DNI	0 Ohm	-15V external supply output jumper
R26, R37	0 Ohm	0 Ohm	DNI	+/-30V supply return jumper to Star GND
C36, C38	10 UF	10 UF	DNI	+/-15V regulator output filter caps
C34, C39	10 UF	DNI	DNI	+/-15V regulator output filter caps
C35, C37	1 UF	1 UF	DNI	+/-15V regulator output filter caps
C29, C30	10 UF	10 UF	DNI	+/-15V regulator input filter caps
C32, C33	1 UF	1 UF	DNI	+/-15V regulator input filter caps

* SN-003 C65 between pin 5 and -12V

APPENDIX A-3
SCHEMATIC REDLINES, SN001

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SAN JOSE, CA 95123
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IC7 AD797R
IC12 OPA549S
IC10 LT1354CS8
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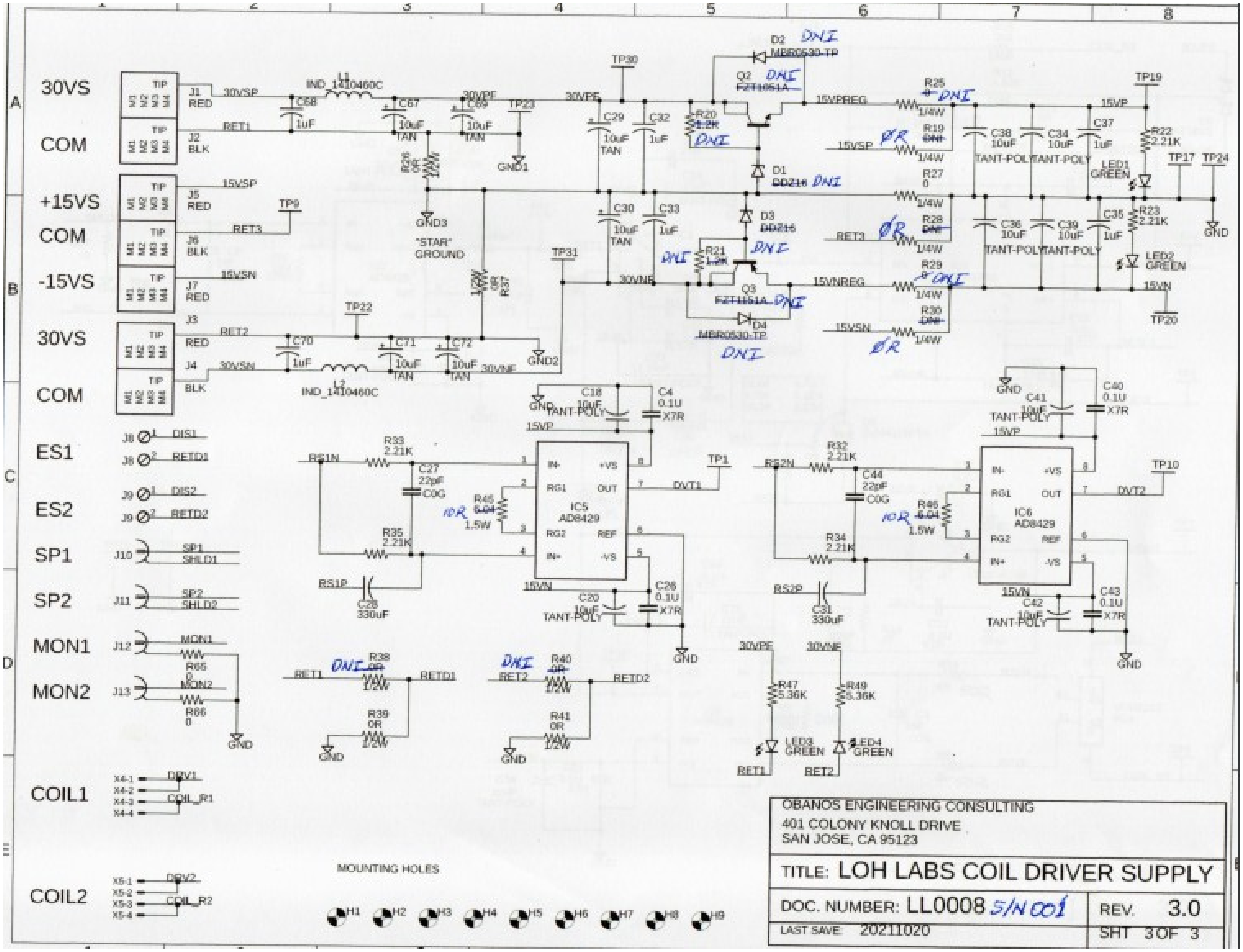
Q4 ZVN4106FTA
D6 BAT160S
RLIM ILIM
4.75K 6.12A
16.5K 3.12A
SHLD2
SP2
SET2
PI2
ICOIL2
MON2
DRV2
ES2
DIS2
RETD2
RET2
COIL_R2
RS2N
RS2P
30VPF
30VNF
15VP
15VN
GND
TP12
TP13
TP14
TP15
TP16
TP26
TP27
TP28
TP29
TP11
R58 0
R50 1k
R60 1k
C64 1nF C0G
R48 DNI 1/4W
C50 10uF TANT-POLY
C46 0.1U X7R
C51 10uF TANT-POLY
C56 0.1U X7R
R43 3.01k 1K
R44 DNI 1M
C45 22pF C0G
C57 0.1U X7R
C53 10uF TANT-POLY
C65 22pF C0G DNI
C55 0.1U X7R
C49 10uF TANT-POLY
R42 100k 50K
C76 22nF C0G
R63 3.01k 1K
R54 4.99K 1/4W
R56 DNI 1/4W
R53 4.99K 1/4W
R52 0R 1/2W
C66 1nF C0G 22NF
C47 10uF TANT-POLY
C58 0.1U X7R
R57 4.75K
C59 0.1U X7R
C48 10uF TANT-POLY
R64 3.01k
C60 0.1U X7R
C61 0.1U X7R
C77 22pF C0G
R59 47
C62 0.1U X7R
C54 10uF TANT-POLY
R51 1/4W DNI
C78 1nF C0G
R61 1k 50R
R62 1k 50R
C52 10uF TANT-POLY
C63 0.1U X7R



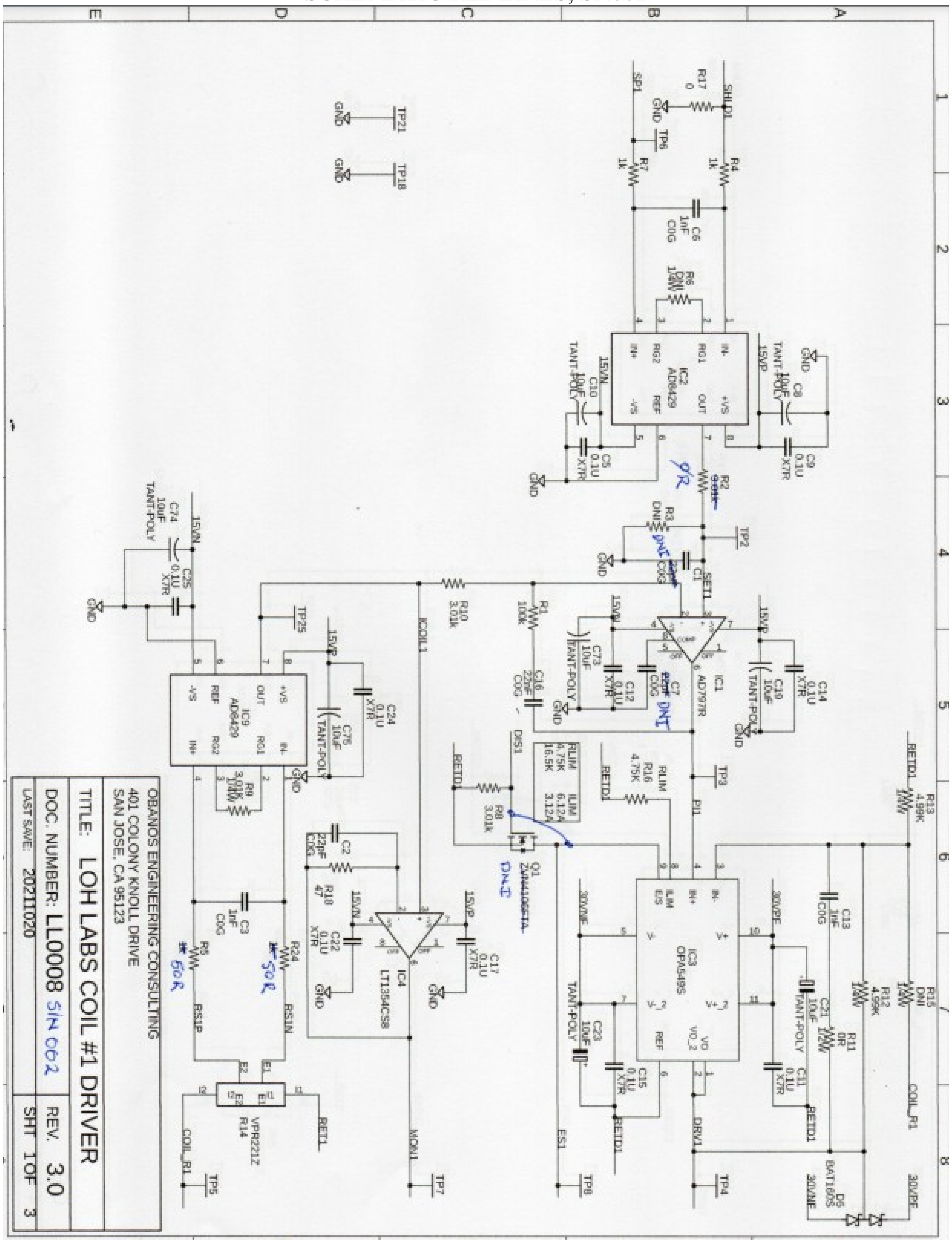
OBANOS ENGINEERING CONSULTING
401 COLONY KNOLL DRIVE
SAN JOSE, CA 95123

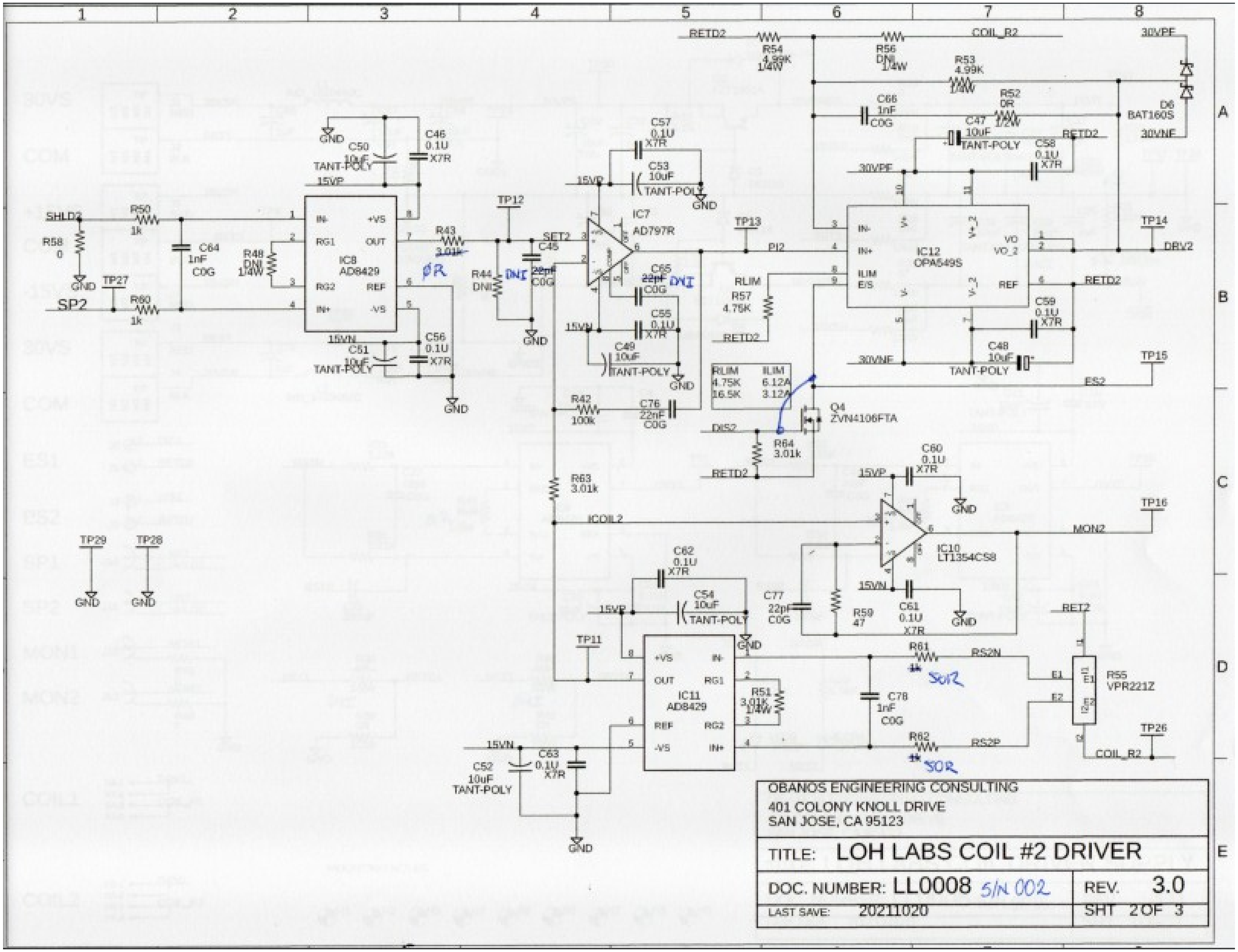
TITLE: LOH LABS COIL DRIVER SUPPLY

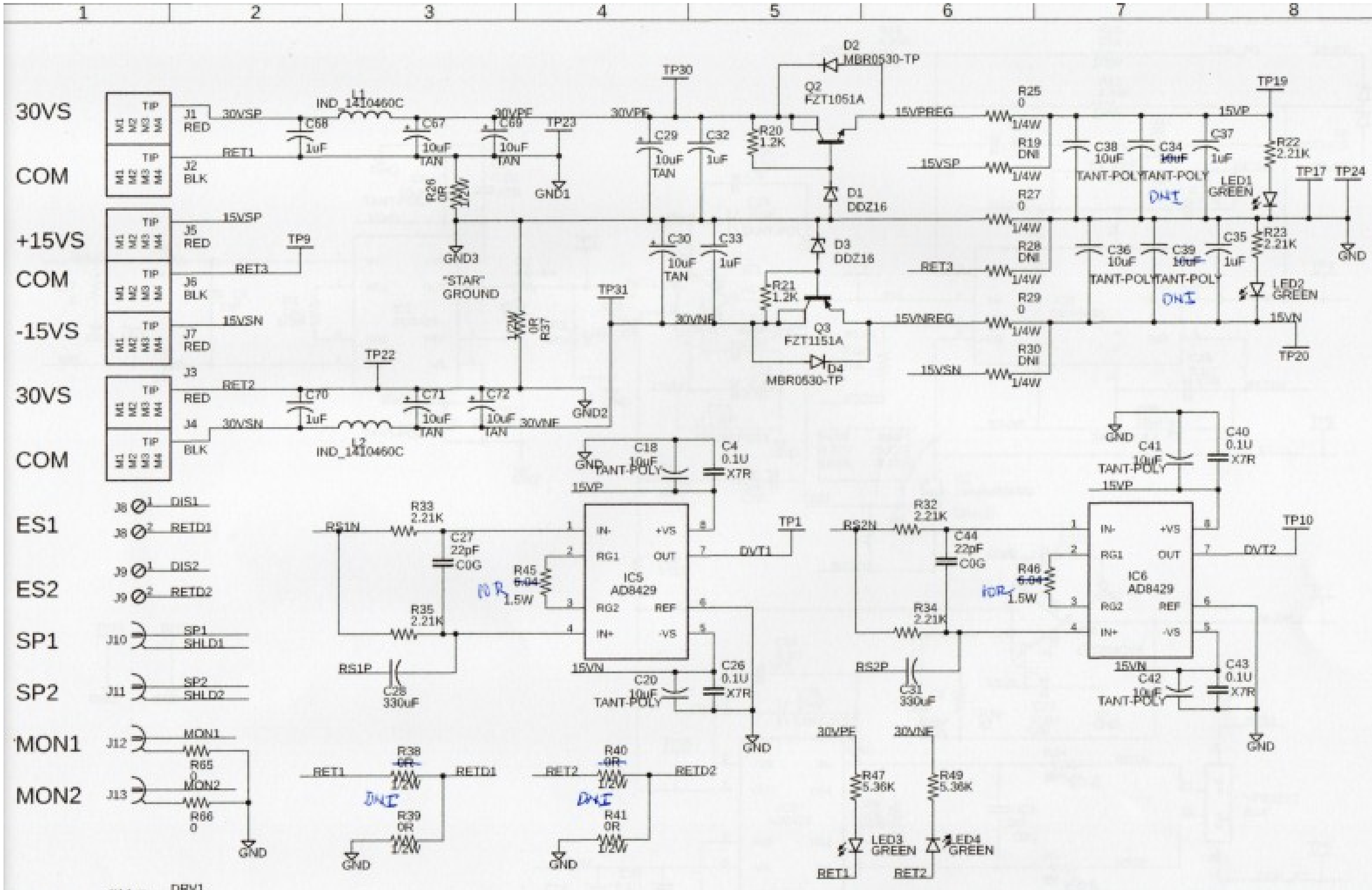
DOC. NUMBER: LL0008 S/N 001 REV. 3.0

LAST SAVE: 20211020 SHT 3 OF 3

SCHEMATIC REDLINES, SN002




OBANOS ENGINEERING CONSULTING
401 COLONY KNOLL DRIVE
SAN JOSE, CA 95123
TITLE: LOH LABS COIL #2 DRIVER
DOC. NUMBER: LL0008 S/N 002
REV. 3.0
LAST SAVE: 20211020
SHT 2 OF 3
IC8 AD8429
IC11 AD8429
IC7 AD797R
IC12 OPA549S
IC10 LT1354CS8
Q4 ZVN4106FTA
D6 BAT160S
R55 VPR221Z
RLIM ILIM
4.75K 6.12A
16.5K 3.12A
SHLD2
SP2
DRV2
MON2
COIL_R2
RETD2
ICOIL2
ES2
DIS2
PI2
SET2
RS2N
RS2P
ØR
DNI
SOR



OBANOS ENGINEERING CONSULTING
401 COLONY KNOLL DRIVE
SAN JOSE, CA 95123

TITLE: LOH LABS COIL DRIVER SUPPLY

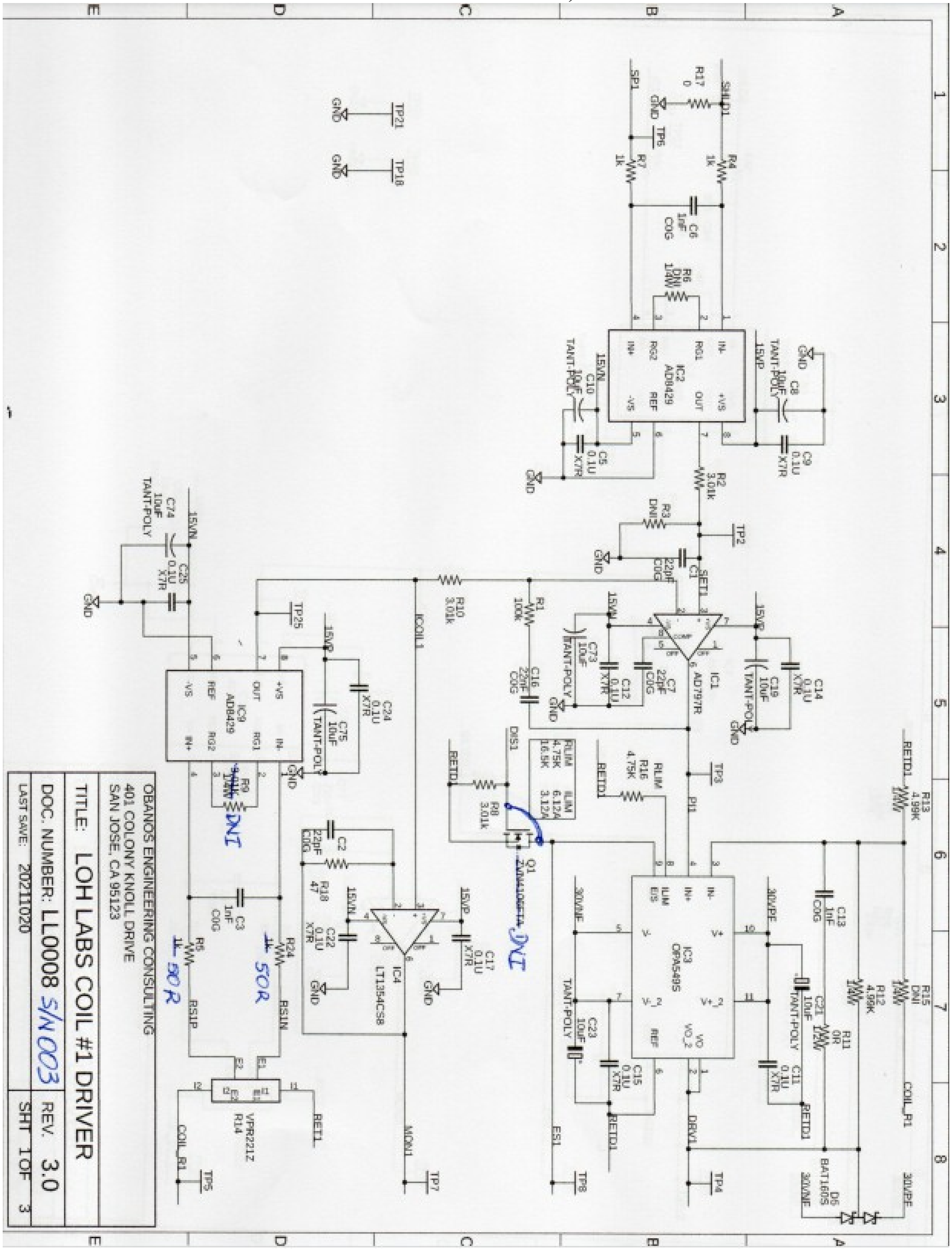
DOC. NUMBER: LL0008 S/N 002

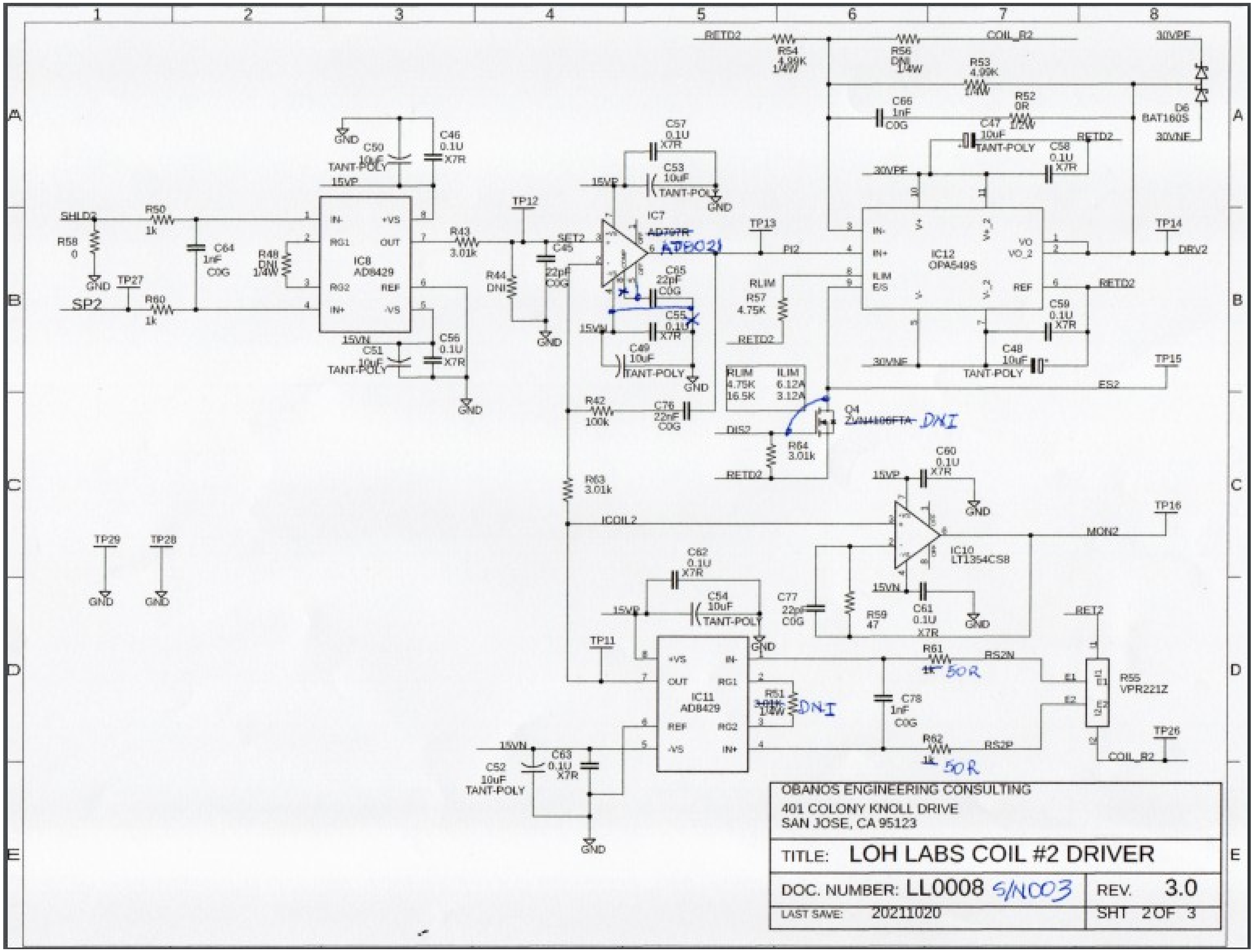
REV. 3.0

LAST SAVE: 20211020

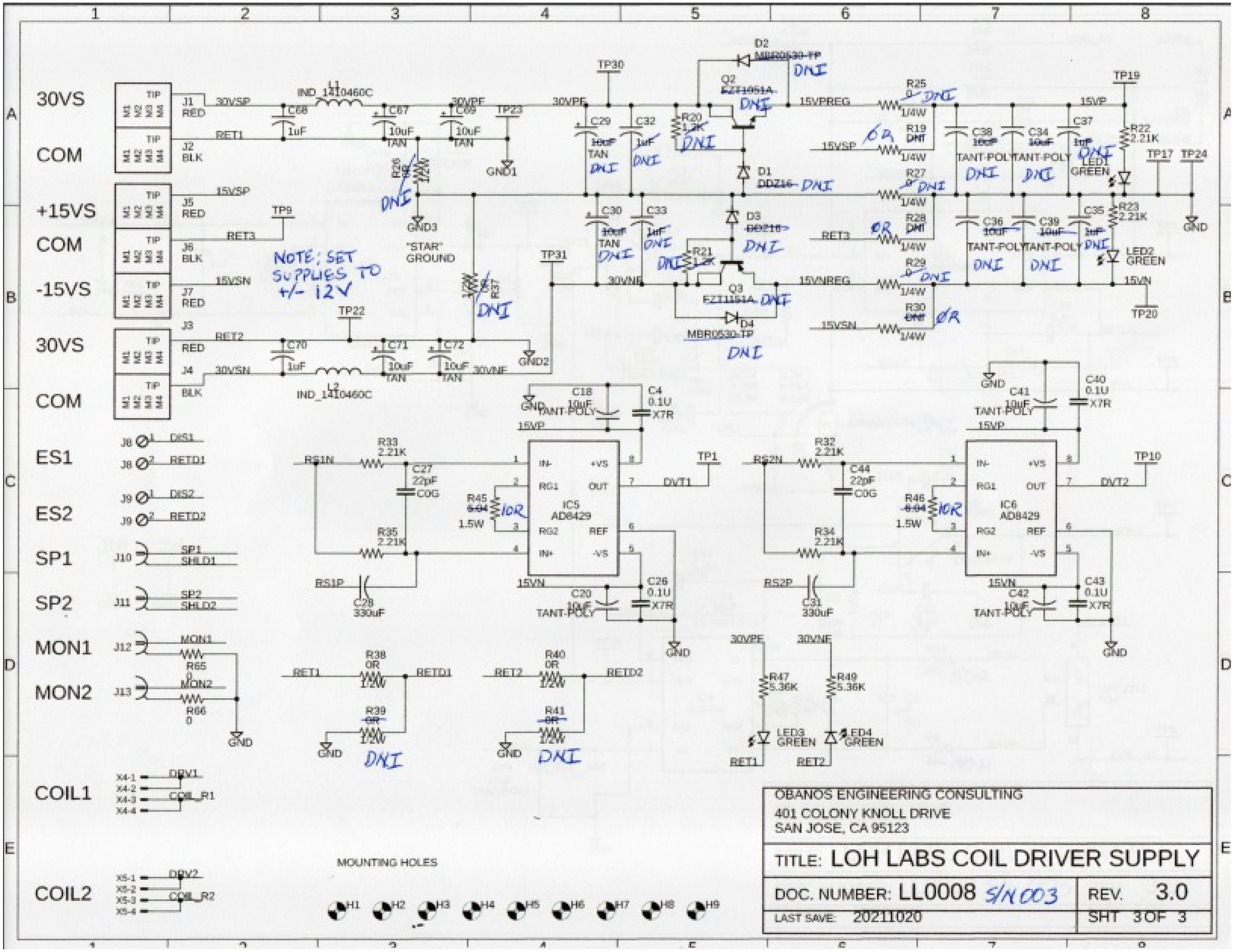
SHT 3 OF 3

SCHEMATIC REDLINES, SN003





OBANOS ENGINEERING CONSULTING 401 COLONY KNOLL DRIVE SAN JOSE, CA 95123		
TITLE:	LOH LABS COIL #2 DRIVER	
DOC. NUMBER:	LL0008 S/N003	REV. 3.0
LAST SAVE:	20211020	SHT 2 OF 3


30VS
COM
+15VS
COM
-15VS
30VS
COM
ES1
ES2
SP1
SP2
MON1
MON2
COIL1
COIL2
NOTE: SET SUPPLIES TO +/- 12V
"STAR" GROUND
IC5 AD8429
IC6 AD8429
MOUNTING HOLES
DNI
OBANOS ENGINEERING CONSULTING
401 COLONY KNOLL DRIVE
SAN JOSE, CA 95123
TITLE: LOH LABS COIL DRIVER SUPPLY
DOC. NUMBER: LL0008 S/N 003
REV. 3.0
LAST SAVE: 20211020
SHT 3 OF 3

APPENDIX B.
PCBA power supply and test coil connections

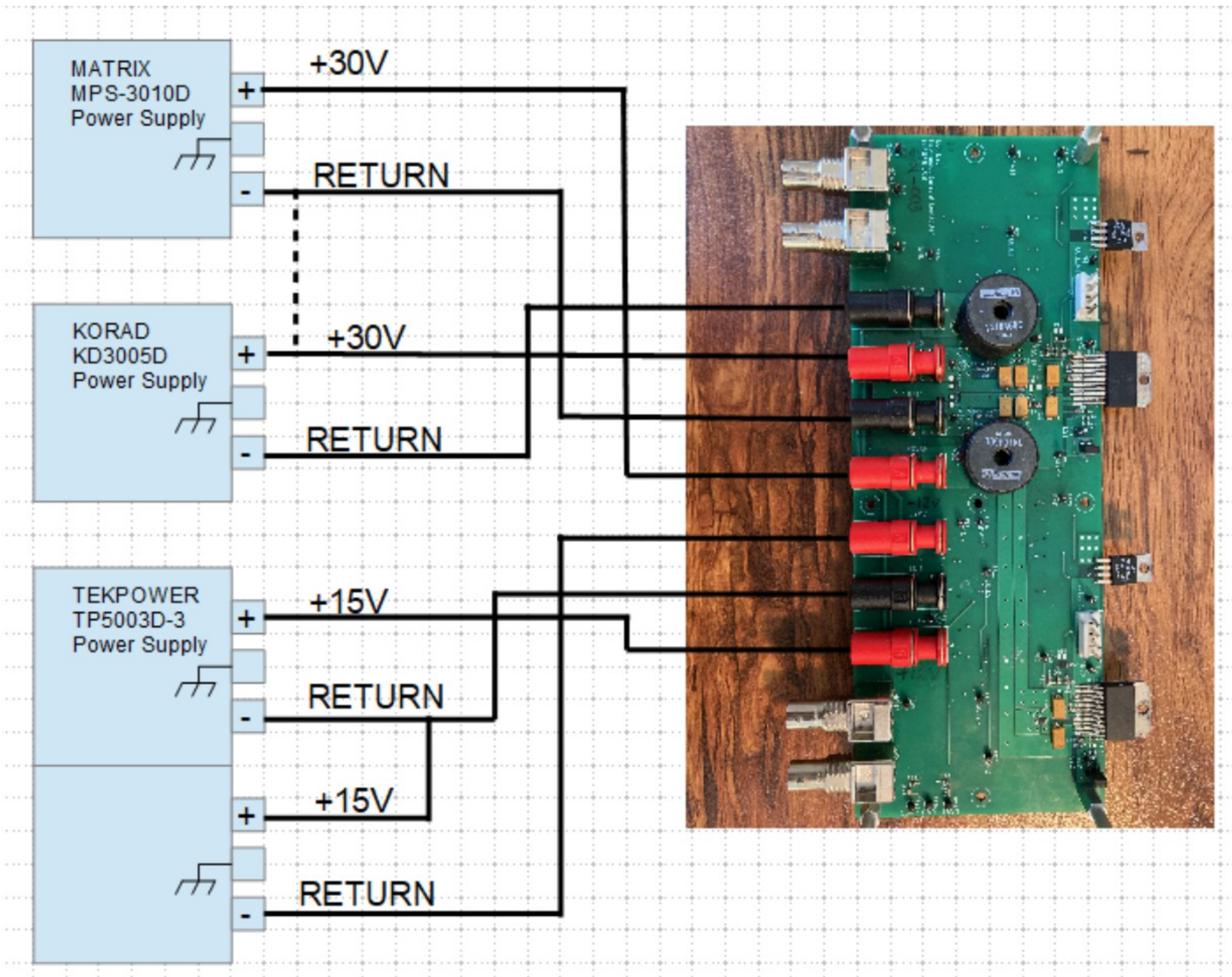


Figure 1. Power supply connections.
(nbvgcfgge

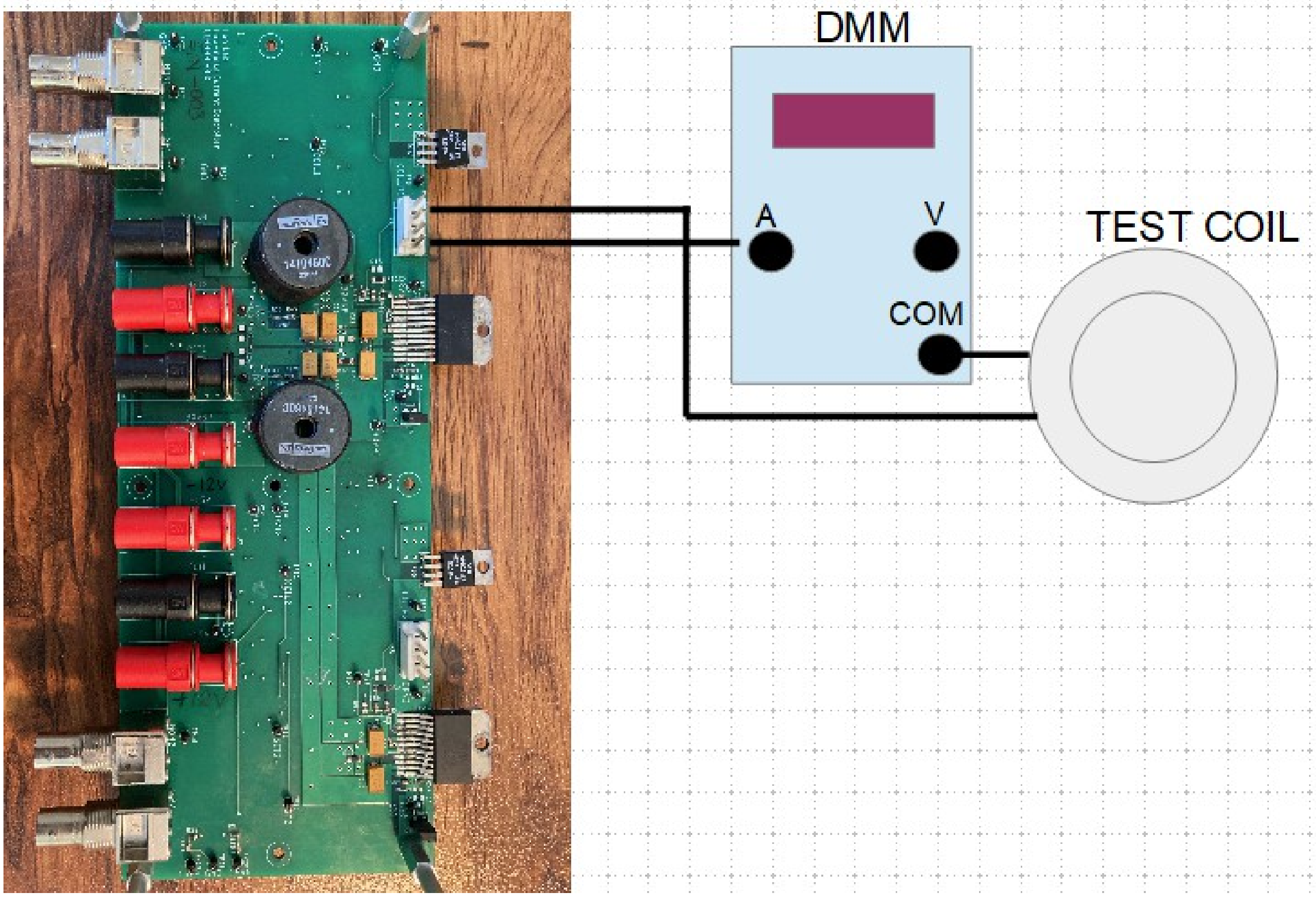
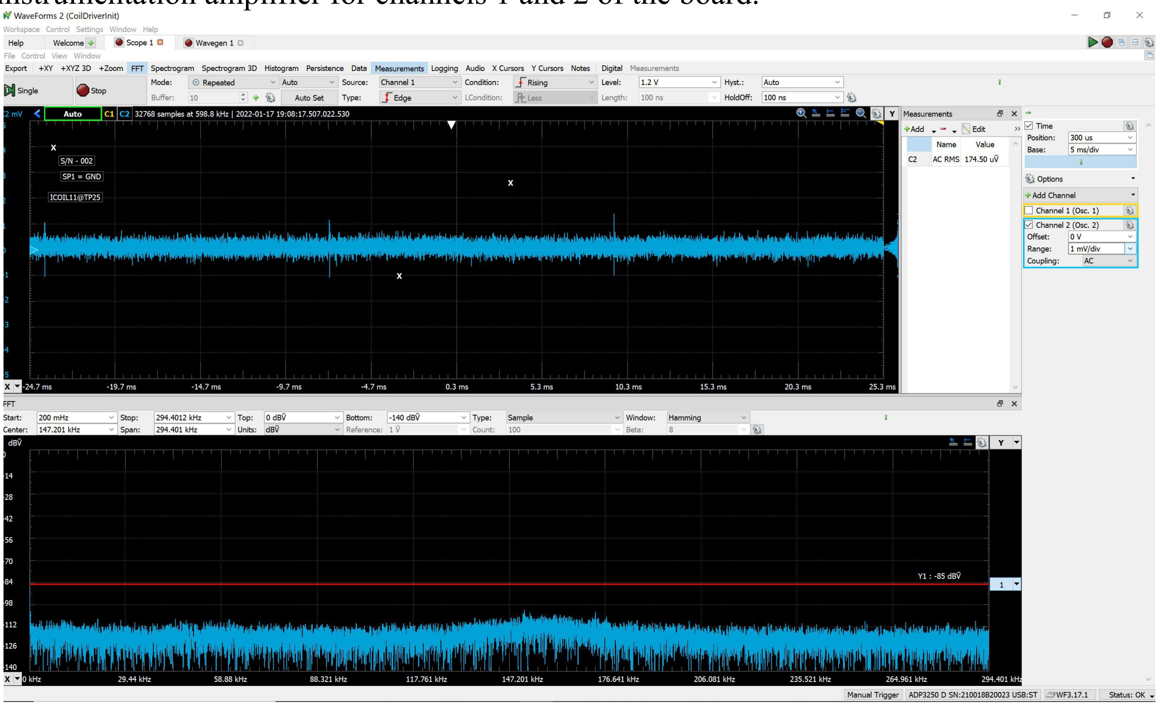


Figure 2. Test coil connected through the DMM.

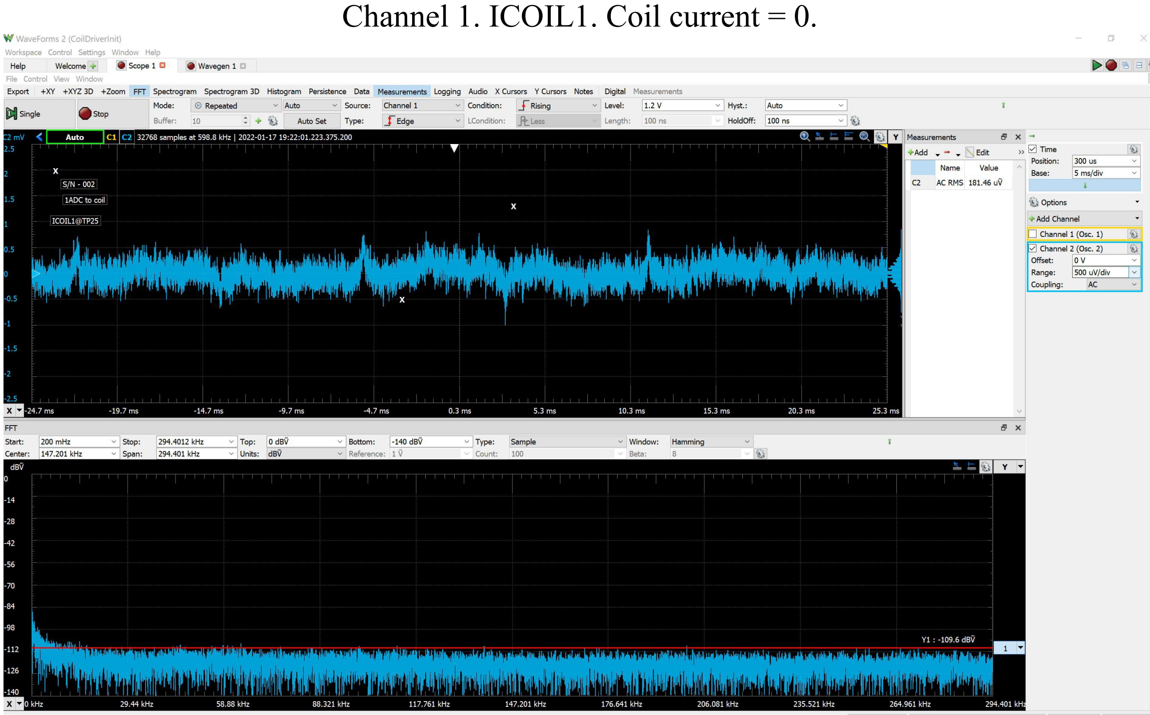
APPENDIX C

Noise waveforms, PCBA S/N -002

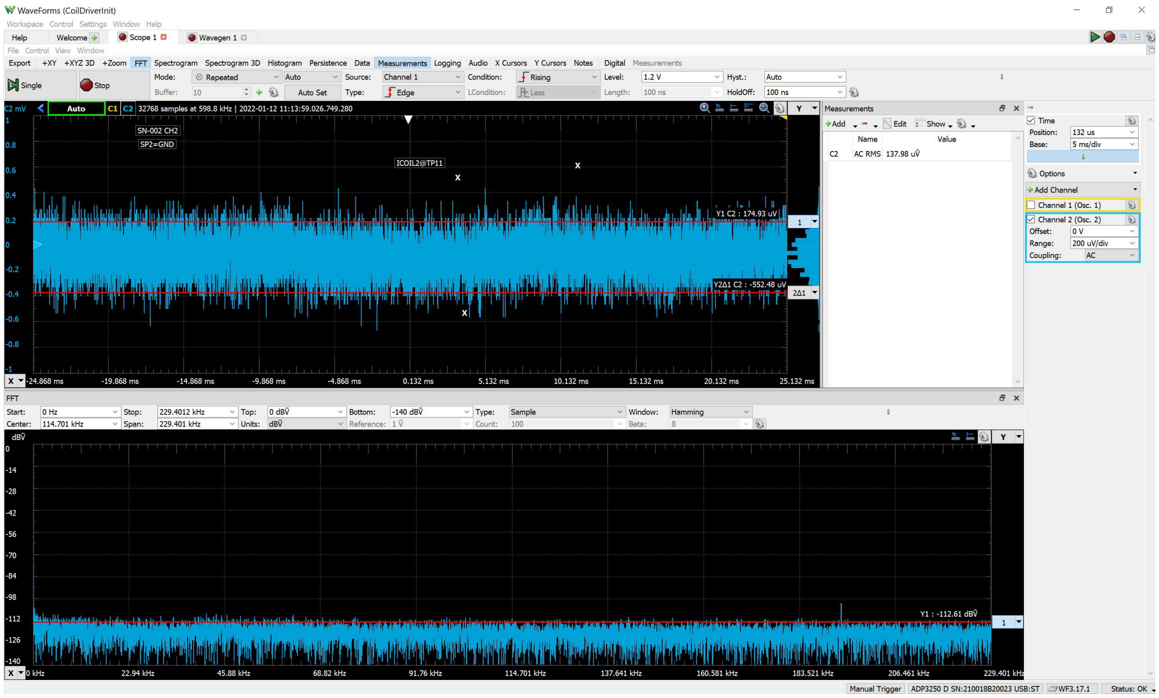
The following oscilloscope screenshots show the voltage at the outputs of the coil current instrumentation amplifier (ICOIL1/2, blue trace) and of the Design Verification Test (DVT1/2, yellow trace) instrumentation amplifier for channels 1 and 2 of the board.



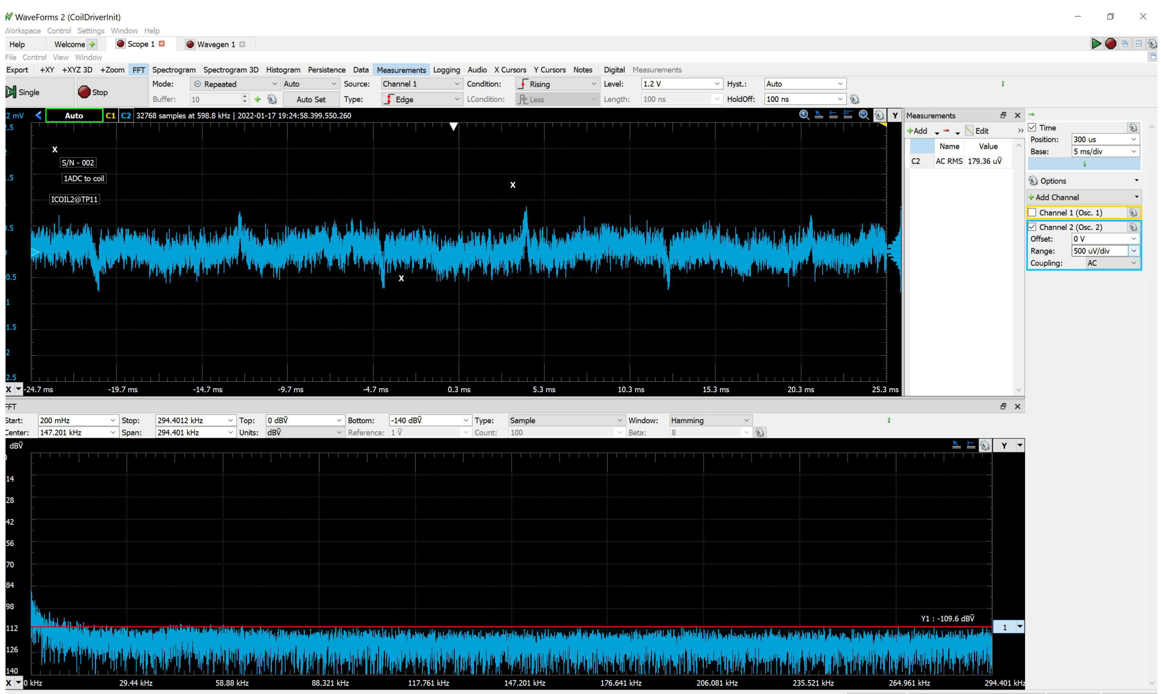
Channel 1. ICOIL1. Coil current = 0.



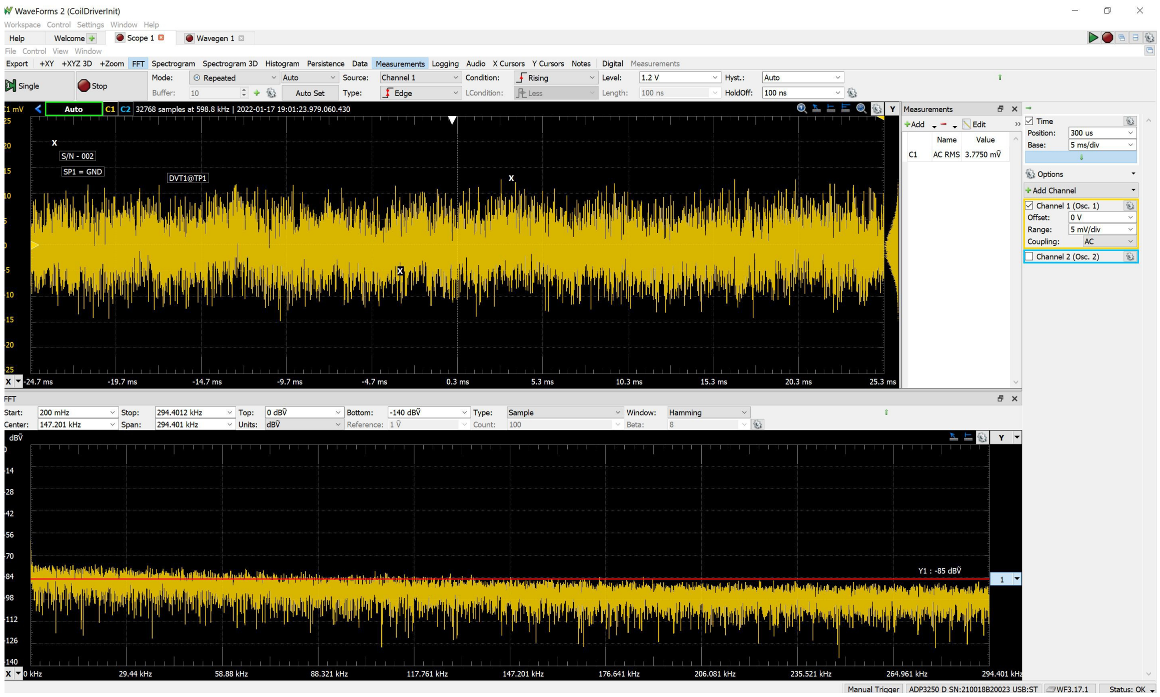
Channel 1. ICOIL1. Coil current = 1A DC



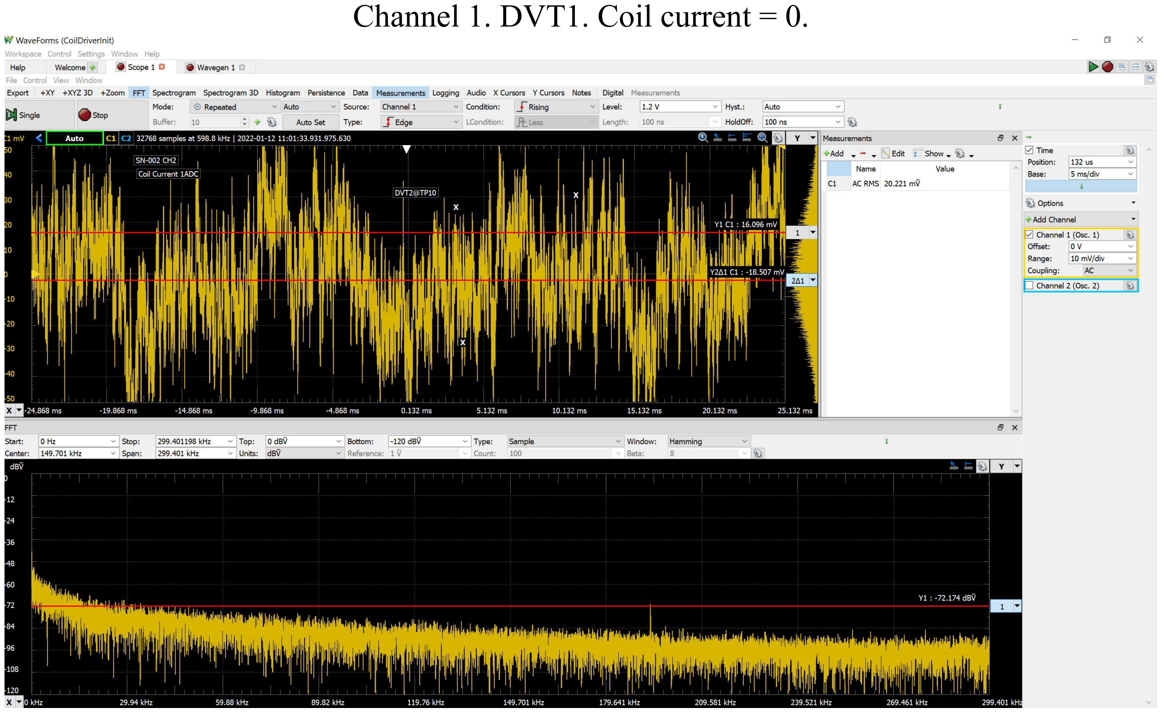
Channel 2. ICOIL2. Coil current = 0.



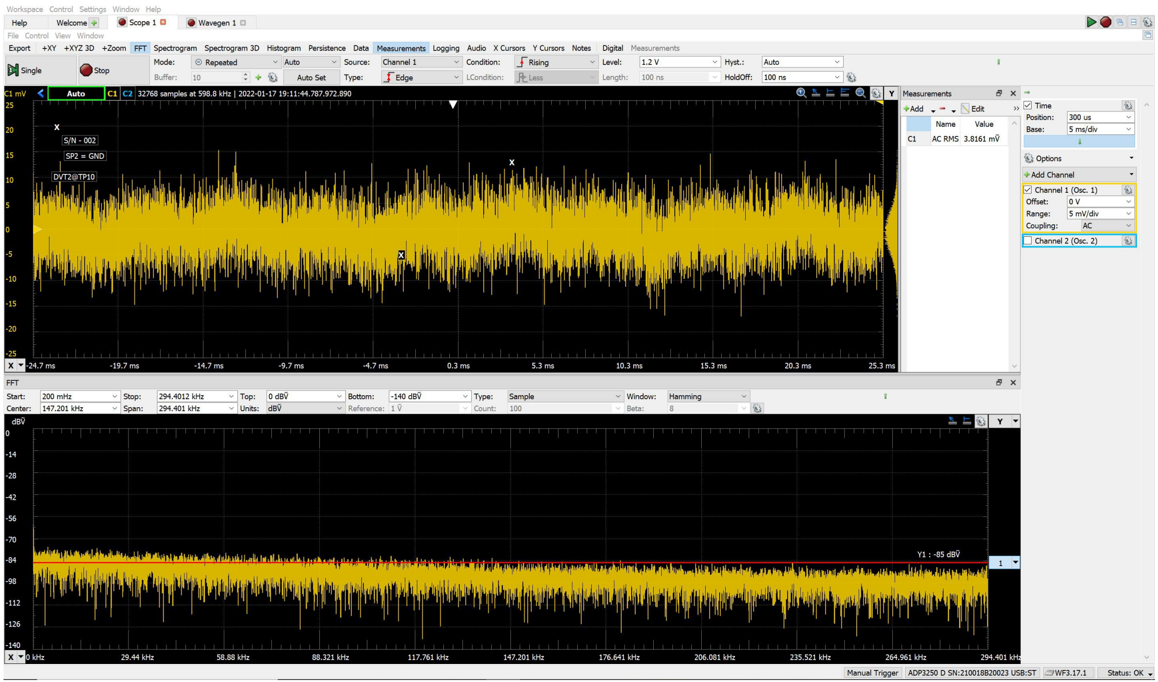
Channel 2. ICOIL2. Coil current = 1A DC.



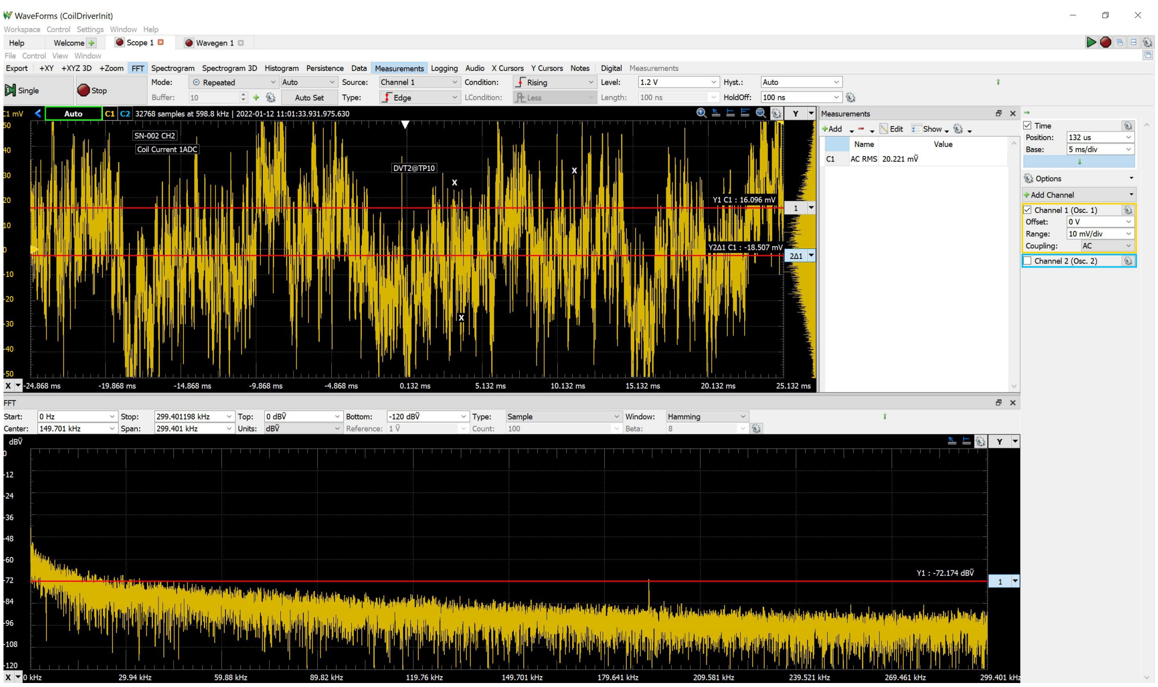
Channel 1. DVT1. Coil current = 0.



Channel 1. DVT1. Coil current = 1A DC.



Channel 2. DVT2. Coil current = 0.



Channel 2. DVT2. Coil current = 1A DC.